FIG.1

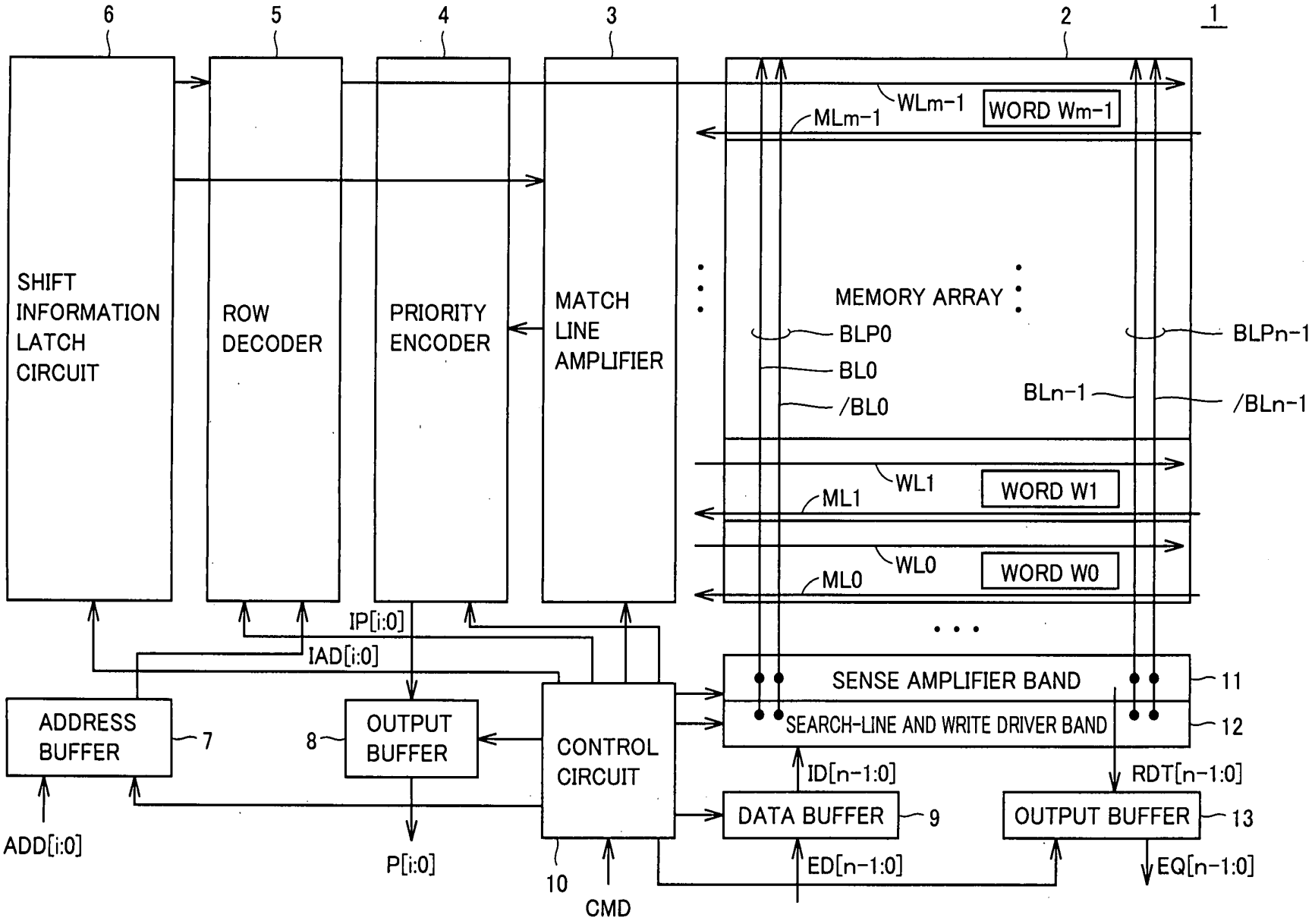

6
5
4
3
2
1
SHIFT INFORMATION LATCH CIRCUIT
ROW DECODER
PRIORITY ENCODER
MATCH LINE AMPLIFIER
MEMORY ARRAY
WLm-1
WORD Wm-1
MLm-1
BLP0
BL0
/BL0
BLPn-1
BLn-1
/BLn-1
WL1
WORD W1
ML1
WL0
WORD W0
ML0
IP[i:0]
IAD[i:0]
SENSE AMPLIFIER BAND
11
SEARCH-LINE AND WRITE DRIVER BAND
12
ADDRESS BUFFER
7
8
OUTPUT BUFFER
CONTROL CIRCUIT
ID[n-1:0]
RDT[n-1:0]
DATA BUFFER
9
OUTPUT BUFFER
13
ADD[i:0]
P[i:0]
10
CMD
ED[n-1:0]
EQ[n-1:0]

FIG.2

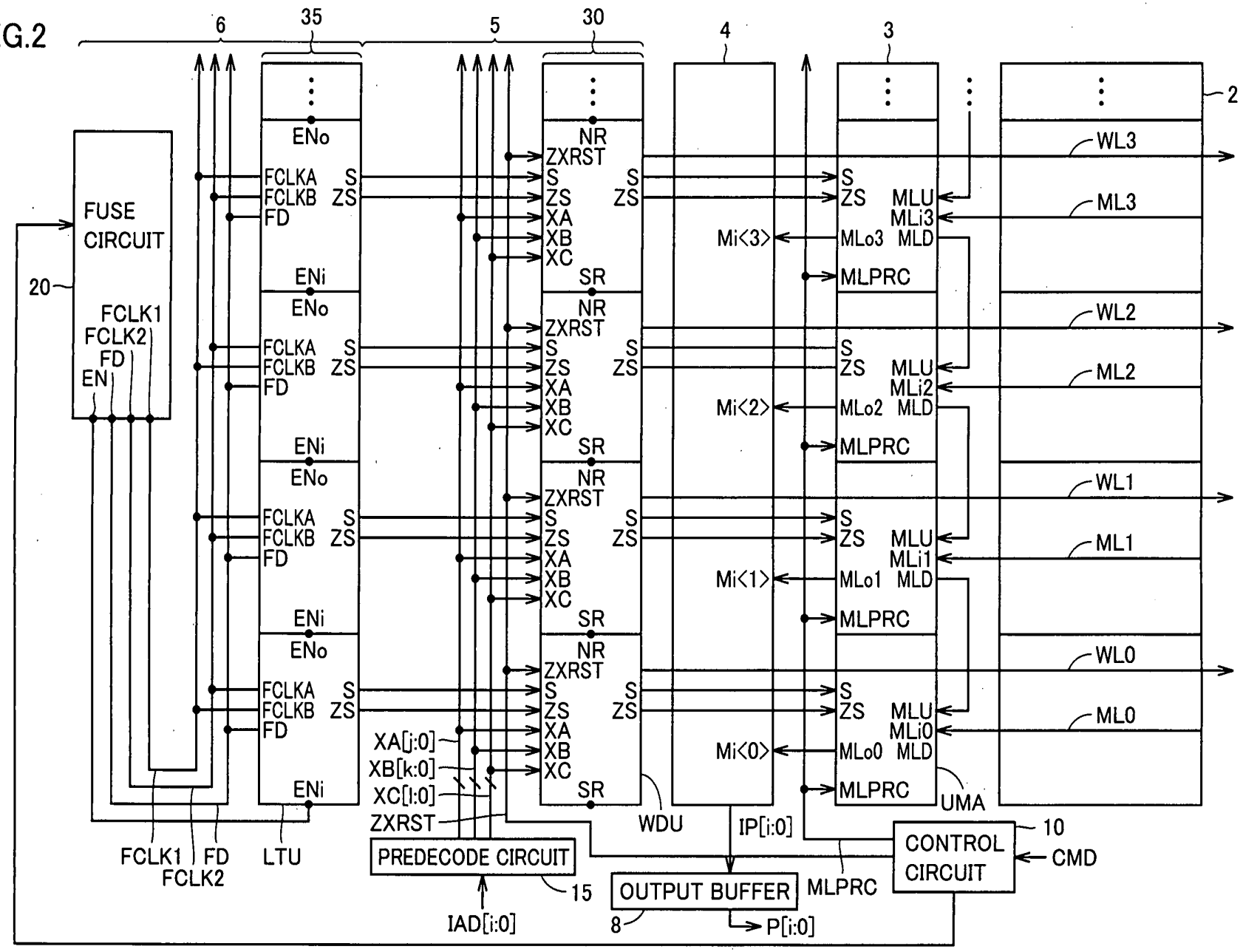

6
35
5
30
4
3
2
FUSE CIRCUIT
20
FCLK1
FCLK2
FD
EN
ENo
ENi
FCLKA
FCLKB
FD
S
ZS
NR
ZXRST
XA
XB
XC
SR
WL3
WL2
WL1
WL0
ML3
ML2
ML1
ML0
MLU
MLi3
MLi2
MLi1
MLi0
MLD
MLPRC
Mi<3>
Mi<2>
Mi<1>
Mi<0>
MLo3
MLo2
MLo1
MLo0
UMA
WDU
IP[i:0]
XA[j:0]
XB[k:0]
XC[l:0]
ZXRST
LTU
PREDECODE CIRCUIT
15
IAD[i:0]
OUTPUT BUFFER
8
P[i:0]
CONTROL CIRCUIT
10
CMD

FIG.3

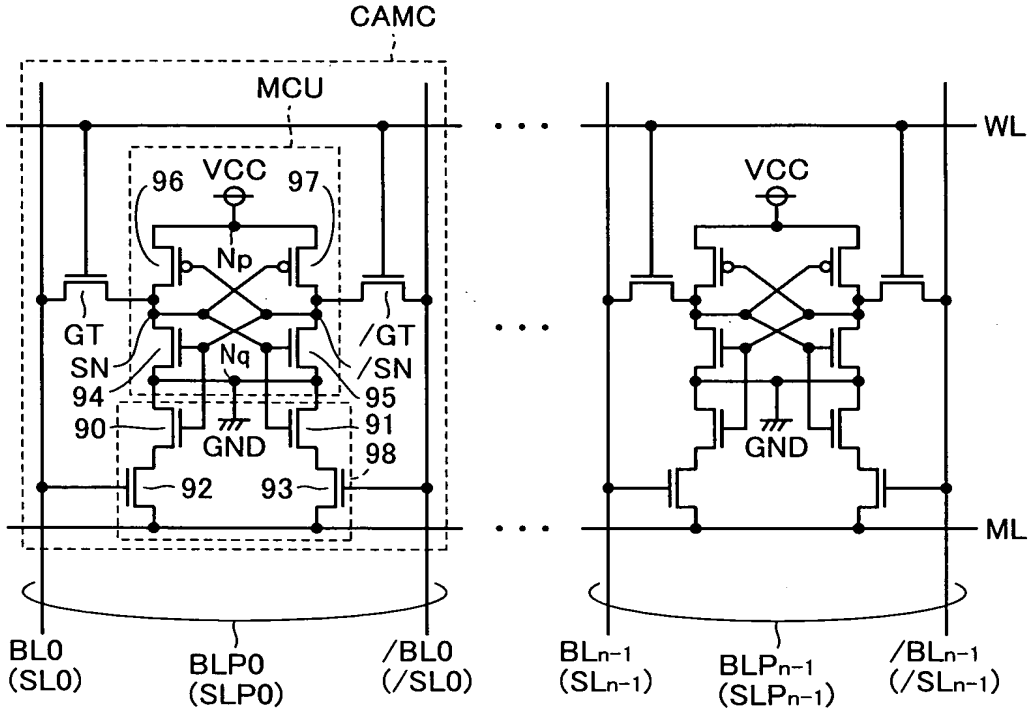

CAMC
MCU
96
VCC
97
Np
GT
SN
94
Nq
/GT
/SN
95
90
GND
91
98
92
93
WL
VCC
GND
ML
BL0
(SL0)
BLP0
(SLP0)
/BL0
(/SL0)
BLn-1
(SLn-1)
BLPn-1
(SLPn-1)
/BLn-1
(/SLn-1)

FIG.4

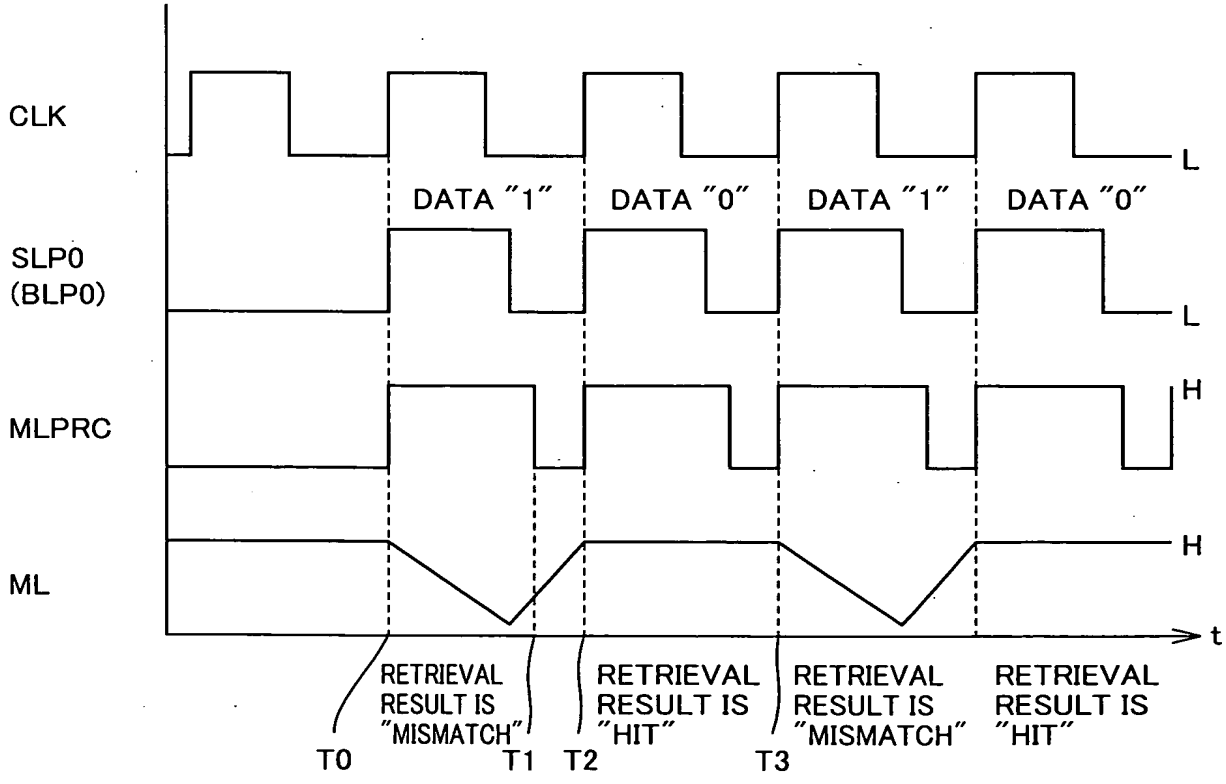

CLK
L
DATA "1"
DATA "0"
DATA "1"
DATA "0"
SLP0
(BLP0)
L
MLPRC
H
ML
H
t
RETRIEVAL RESULT IS "MISMATCH"
RETRIEVAL RESULT IS "HIT"
RETRIEVAL RESULT IS "MISMATCH"
RETRIEVAL RESULT IS "HIT"
T0
T1
T2
T3

FIG.5

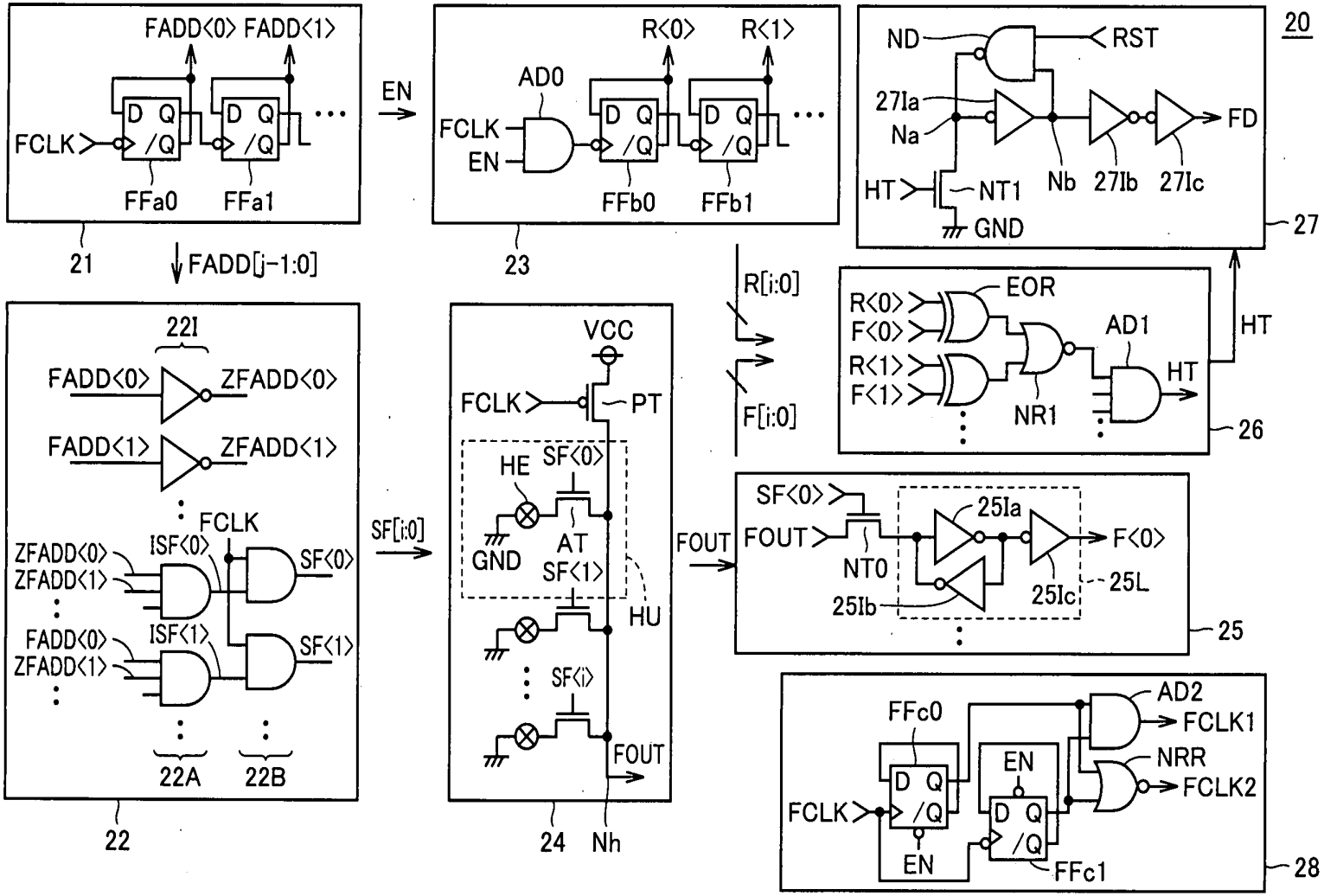

FADD<0>
FADD<1>
FCLK
D Q
/Q
FFa0
FFa1
21
FADD[j-1:0]
EN
R<0>
R<1>
AD0
EN
FFb0
FFb1
23
20
ND
RST
27Ia
Na
FD
HT
NT1
Nb
27Ib
27Ic
GND
27
R[i:0]
F[i:0]
EOR
AD1
HT
NR1
26
22I
ZFADD<0>
ZFADD<1>
ISF<0>
ISF<1>
SF<0>
SF<1>
22A
22B
22
SF[i:0]
VCC
PT
HE
AT
GND
HU
SF<i>
FOUT
24
Nh
SF<0>
25Ia
F<0>
NT0
25Ib
25Ic
25L
25
FFc0
AD2
FCLK1
NRR
FCLK2
FFc1
28

FIG.6

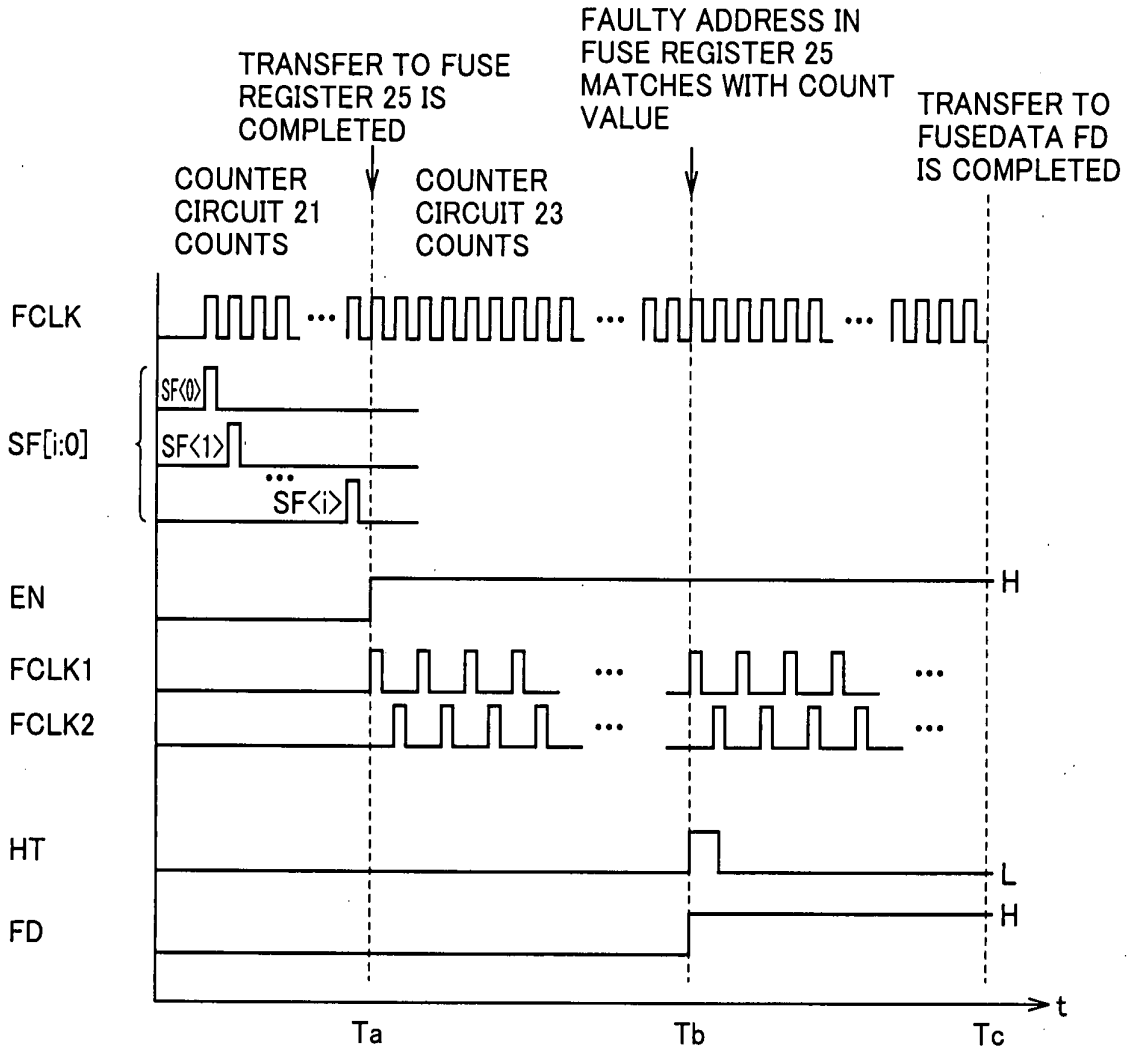

TRANSFER TO FUSE REGISTER 25 IS COMPLETED
FAULTY ADDRESS IN FUSE REGISTER 25 MATCHES WITH COUNT VALUE
TRANSFER TO FUSEDATA FD IS COMPLETED
COUNTER CIRCUIT 21 COUNTS
COUNTER CIRCUIT 23 COUNTS
FCLK
SF[i:0]
SF<0>
SF<1>
SF<i>
EN
H
FCLK1
FCLK2
HT
L
FD
H
t
Ta
Tb
Tc

FIG.7

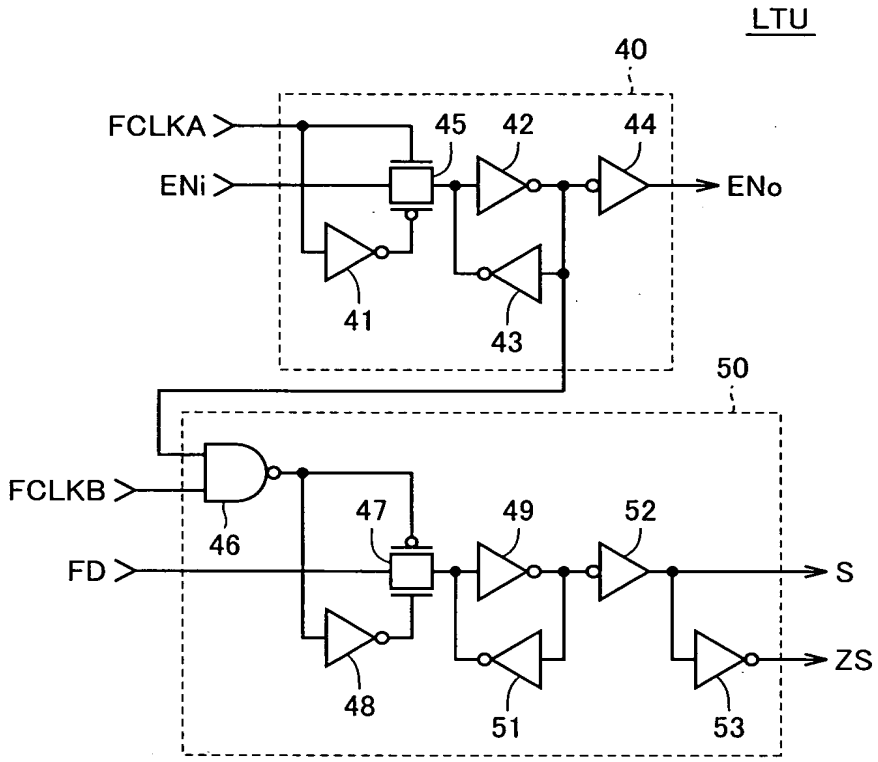

LTU
40
FCLKA
ENi
45
42
44
ENo
41
43
50
FCLKB
46
47
49
52
FD
S
ZS
48
51
53

FIG.8

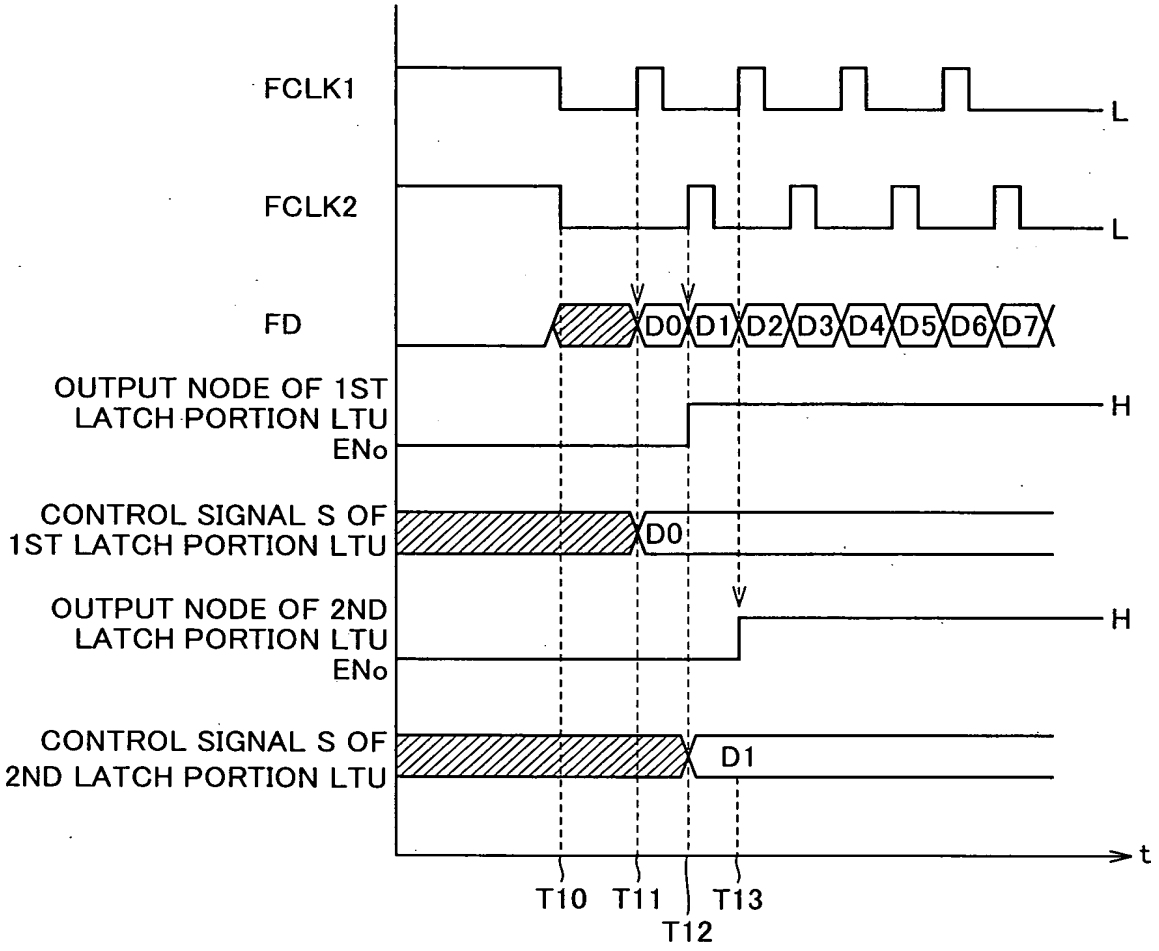

FCLK1
L
FCLK2
L
FD
D0
D1
D2
D3
D4
D5
D6
D7
OUTPUT NODE OF 1ST LATCH PORTION LTU ENo
H
CONTROL SIGNAL S OF 1ST LATCH PORTION LTU
D0
OUTPUT NODE OF 2ND LATCH PORTION LTU ENo
H
CONTROL SIGNAL S OF 2ND LATCH PORTION LTU
D1
t
T10
T11
T12
T13

FIG.9

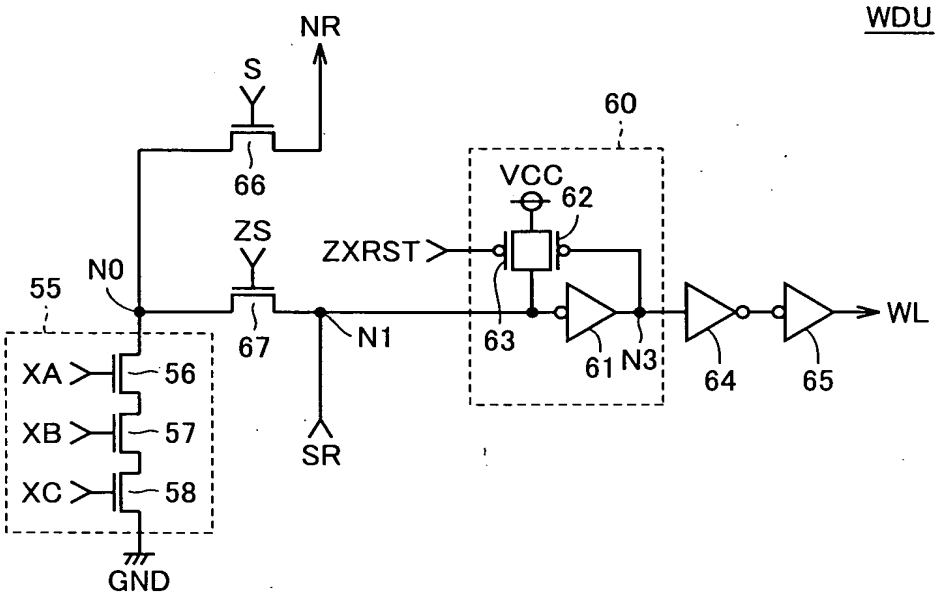

WDU
NR
S
66
60
VCC
62
ZS
ZXRST
N0
55
67
N1
63
61
N3
64
65
WL
XA
56
XB
57
XC
58
SR
GND

FIG.10

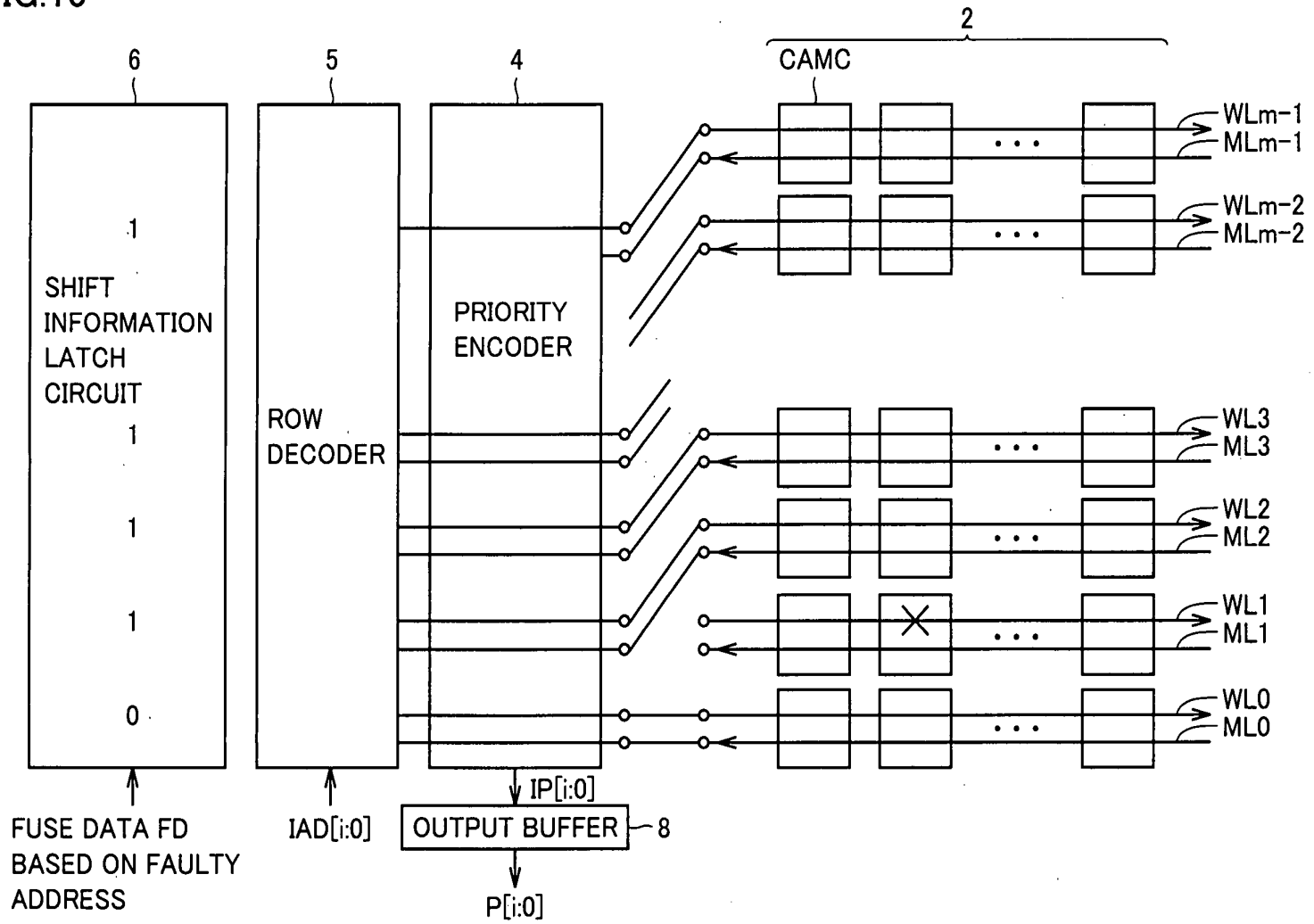

2
CAMC
6
5
4
SHIFT INFORMATION LATCH CIRCUIT
1
1
1
1
0
ROW DECODER
PRIORITY ENCODER
WLm-1
MLm-1
WLm-2
MLm-2
WL3
ML3
WL2
ML2
WL1
ML1
WL0
ML0
IP[i:0]
FUSE DATA FD BASED ON FAULTY ADDRESS
IAD[i:0]
OUTPUT BUFFER
8
P[i:0]

FIG.11

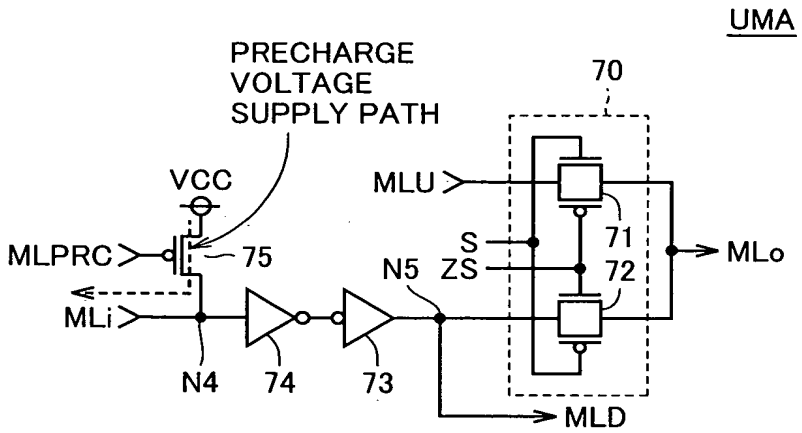

UMA
PRECHARGE
VOLTAGE
SUPPLY PATH
70
VCC
MLU
MLPRC
75
S
71
MLo
N5
ZS
72
MLi
N4
74
73
MLD

FIG.12

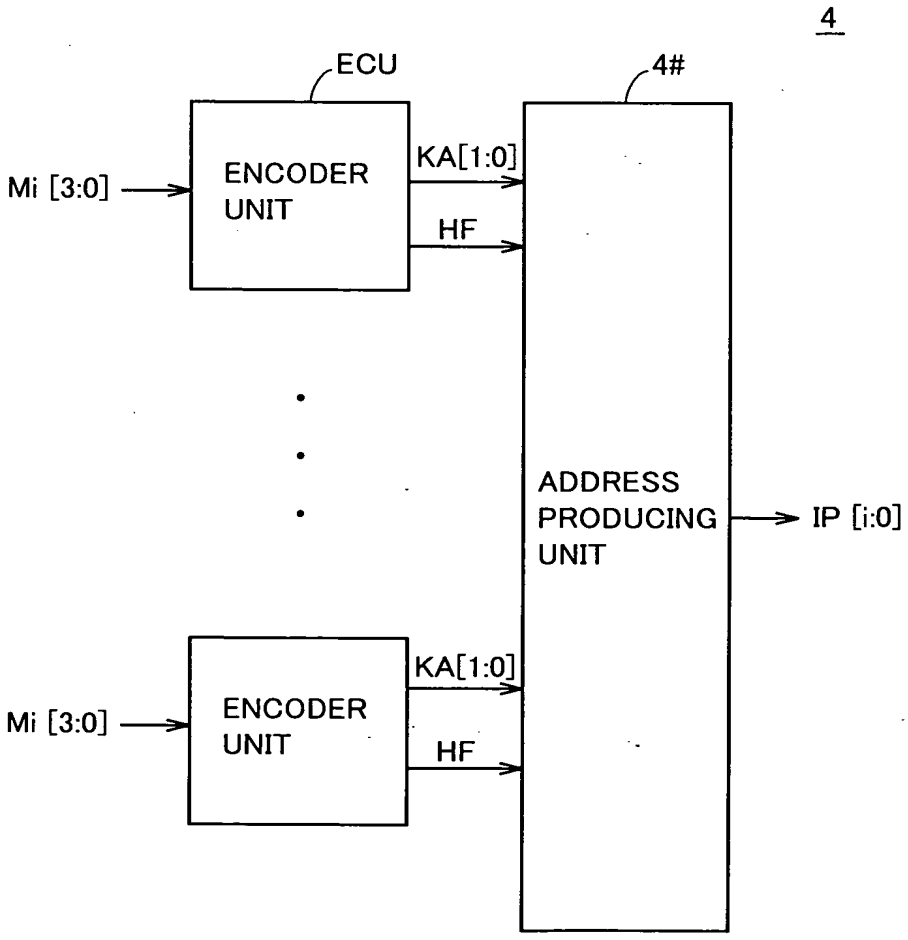

4
ECU
4#
Mi [3:0]
ENCODER
UNIT
KA[1:0]
HF
ADDRESS
PRODUCING
UNIT
IP [i:0]
Mi [3:0]
ENCODER
UNIT
KA[1:0]
HF

FIG.13

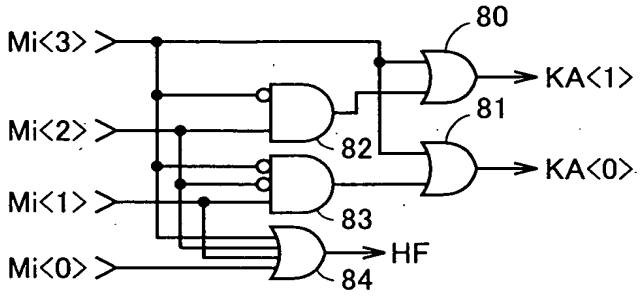


FIG.14

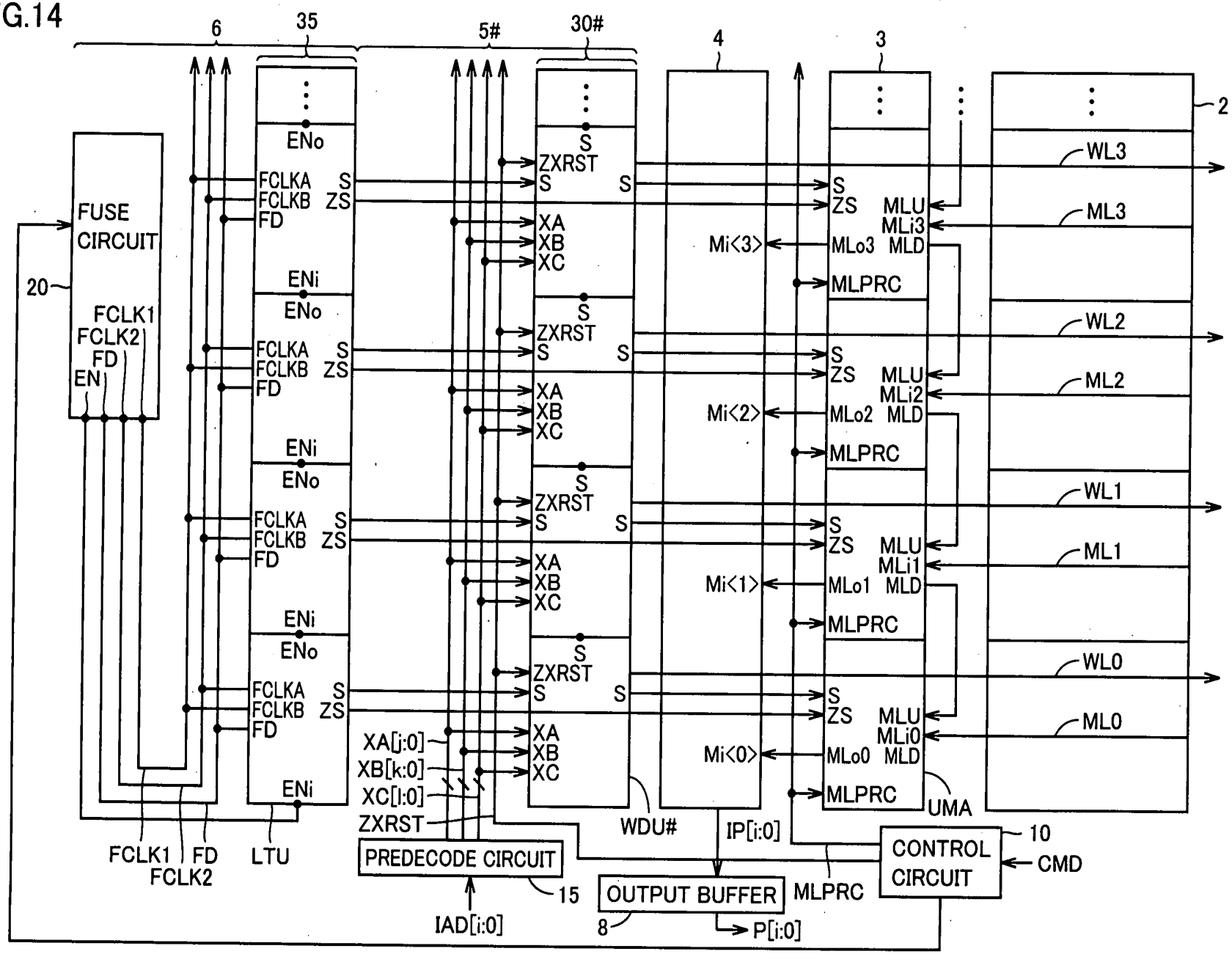

6
35
5#
30#
4
3
2
FUSE CIRCUIT
20
FCLK1
FCLK2
FD
EN
ENo
ENi
FCLKA
FCLKB
FD
S
ZS
ZXRST
XA
XB
XC
MLU
MLi3
MLi2
MLi1
MLi0
MLo3
MLo2
MLo1
MLo0
MLD
MLPRC
Mi<3>
Mi<2>
Mi<1>
Mi<0>
WL3
WL2
WL1
WL0
ML3
ML2
ML1
ML0
UMA
XA[j:0]
XB[k:0]
XC[l:0]
ZXRST
WDU#
IP[i:0]
LTU
PREDECODE CIRCUIT
15
IAD[i:0]
OUTPUT BUFFER
8
P[i:0]
CONTROL CIRCUIT
10
CMD

FIG.15

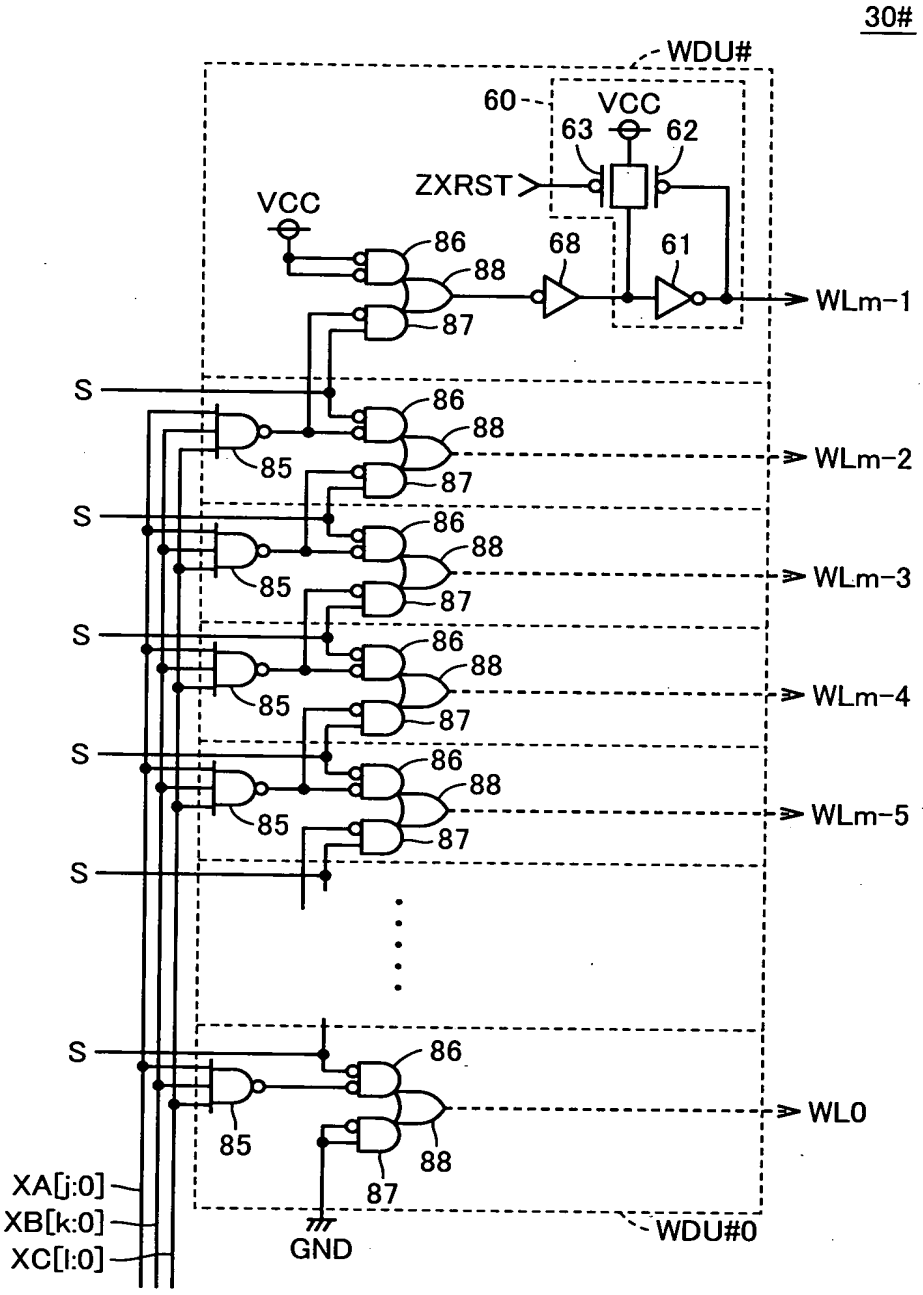

30#
WDU#
60
VCC
63
62
ZXRST
VCC
86
88
87
68
61
WLm-1
S
85
WLm-2
WLm-3
WLm-4
WLm-5
WL0
XA[j:0]
XB[k:0]
XC[l:0]
GND
WDU#0

FIG.16

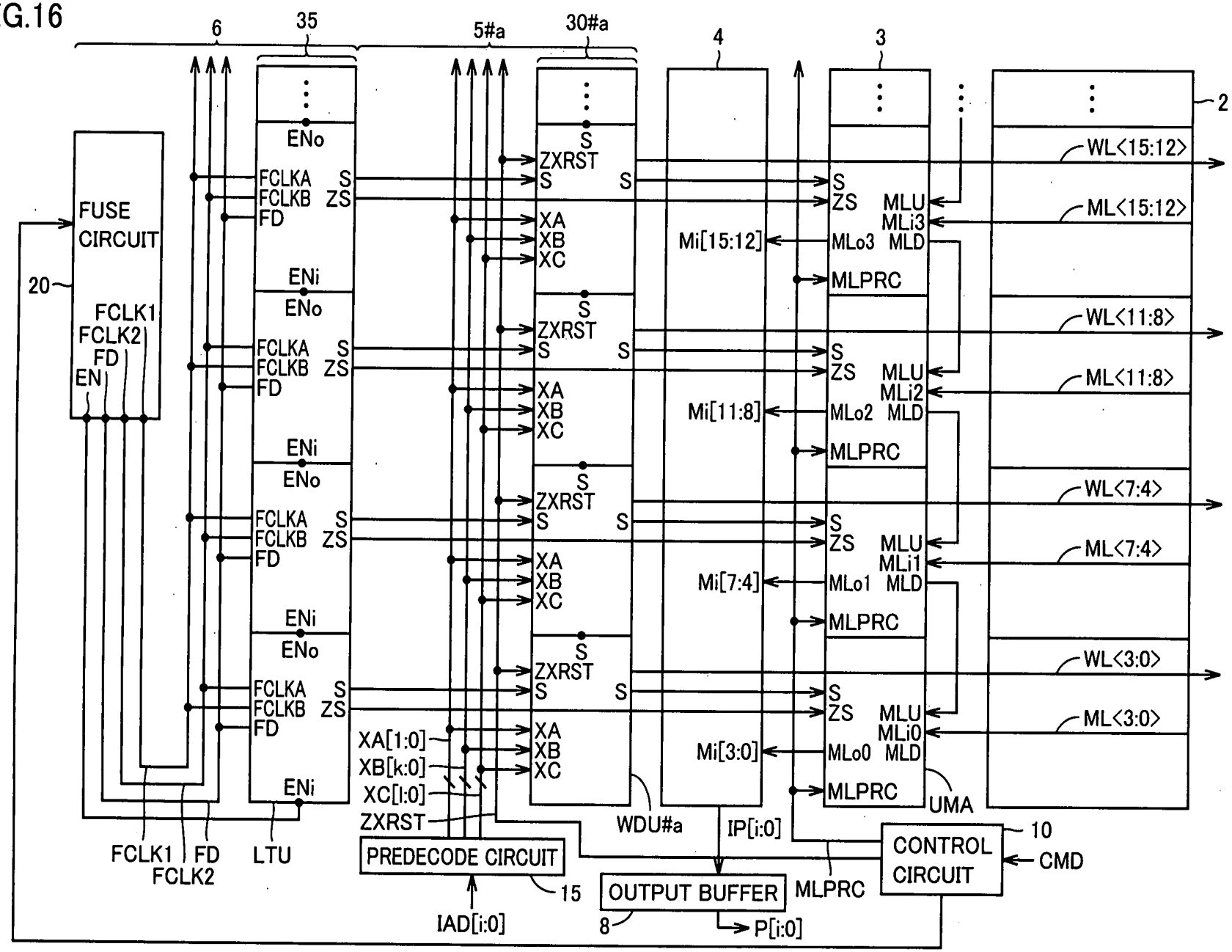

6
35
5#a
30#a
4
3
2
FUSE CIRCUIT
20
FCLK1
FCLK2
FD
EN
ENo
ENi
FCLKA
FCLKB
FD
S
ZS
ZXRST
XA
XB
XC
MLU
MLi3
MLi2
MLi1
MLi0
MLo3
MLo2
MLo1
MLo0
MLD
MLPRC
Mi[15:12]
Mi[11:8]
Mi[7:4]
Mi[3:0]
WL<15:12>
ML<15:12>
WL<11:8>
ML<11:8>
WL<7:4>
ML<7:4>
WL<3:0>
ML<3:0>
XA[1:0]
XB[k:0]
XC[l:0]
ZXRST
FCLK1
FCLK2
FD
LTU
WDU#a
IP[i:0]
UMA
PREDECODE CIRCUIT
15
IAD[i:0]
OUTPUT BUFFER
8
P[i:0]
MLPRC
CONTROL CIRCUIT
10
CMD

FIG.17

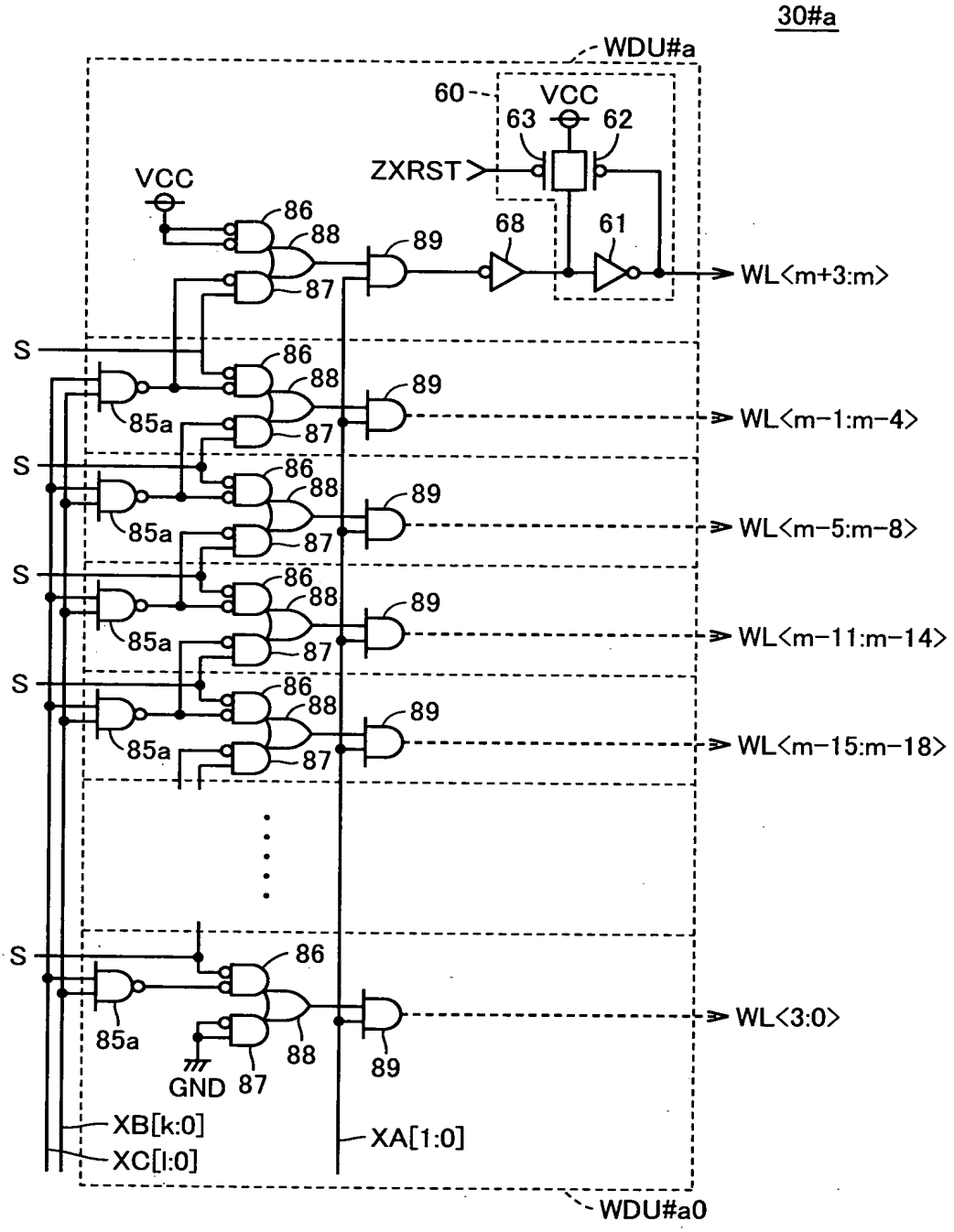

30#a
WDU#a
60
VCC
63
62
ZXRST
68
61
VCC
86
88
89
87
WL<m+3:m>
S
85a
WL<m-1:m-4>
WL<m-5:m-8>
WL<m-11:m-14>
WL<m-15:m-18>
WL<3:0>
GND
XB[k:0]
XC[l:0]
XA[1:0]
WDU#a0

FIG.18

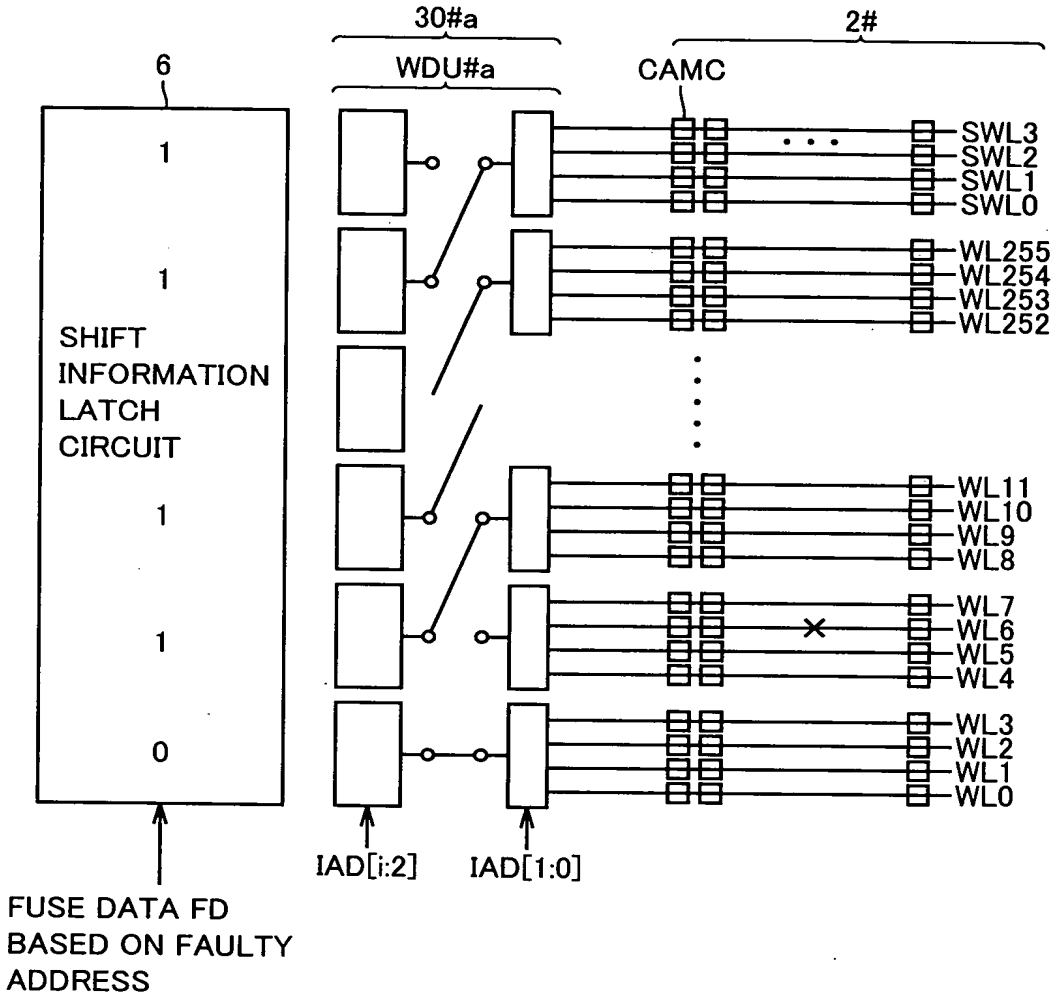

30#a
2#
6
WDU#a
CAMC
1
1
SHIFT
INFORMATION
LATCH
CIRCUIT
1
1
0
SWL3
SWL2
SWL1
SWL0
WL255
WL254
WL253
WL252
WL11
WL10
WL9
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
WL0
IAD[i:2]
IAD[1:0]
FUSE DATA FD
BASED ON FAULTY
ADDRESS

FIG.19

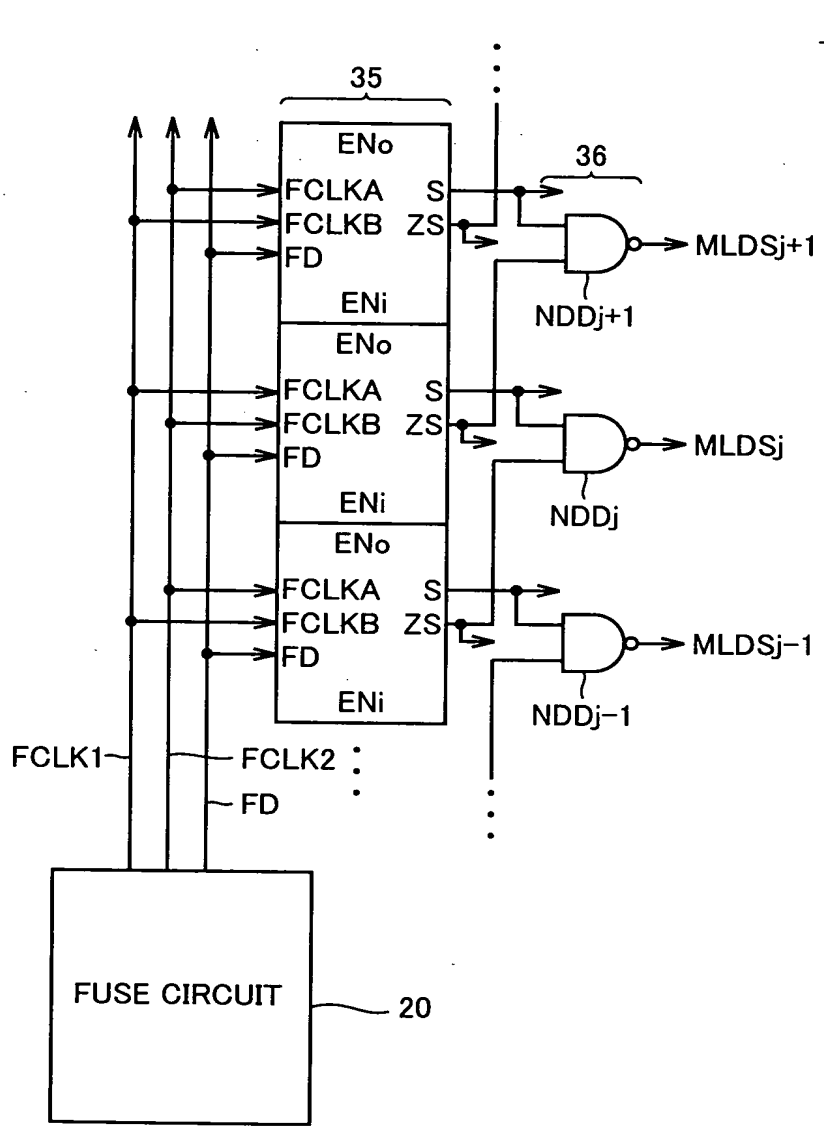

6#
35
36
ENo
FCLKA
FCLKB
FD
S
ZS
ENi
MLDSj+1
NDDj+1
MLDSj
NDDj
MLDSj-1
NDDj-1
FCLK1
FCLK2
FD
FUSE CIRCUIT
20

FIG.20

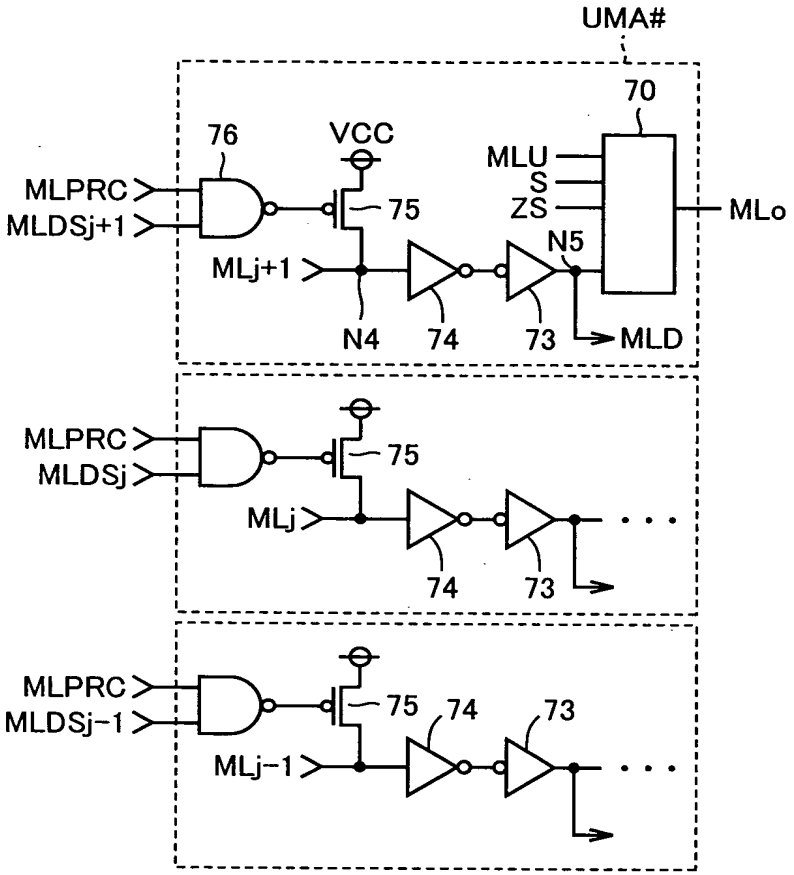

UMA#
70
76
VCC
MLU
S
ZS
MLo
MLPRC
MLDSj+1
75
N5
MLj+1
N4
74
73
MLD
MLPRC
MLDSj
75
MLj
74
73
MLPRC
MLDSj-1
75
74
73
MLj-1

FIG.21

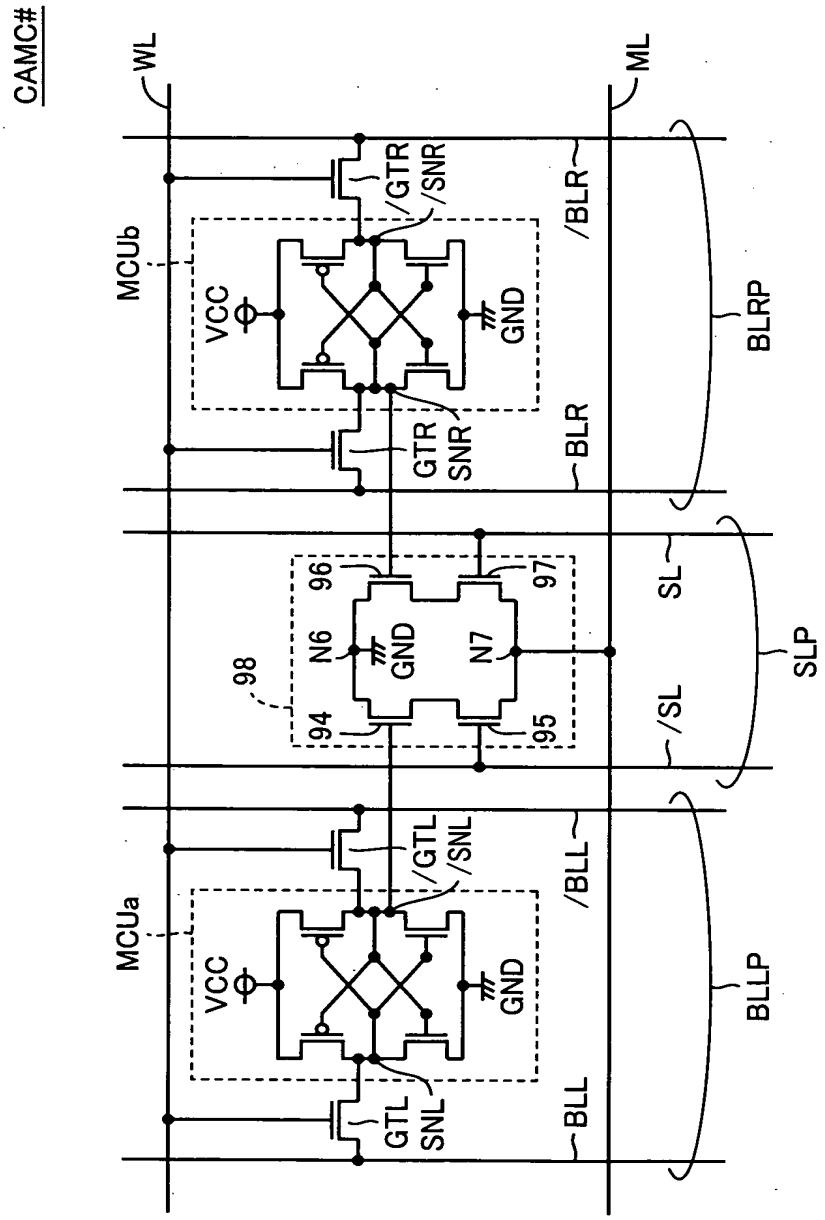
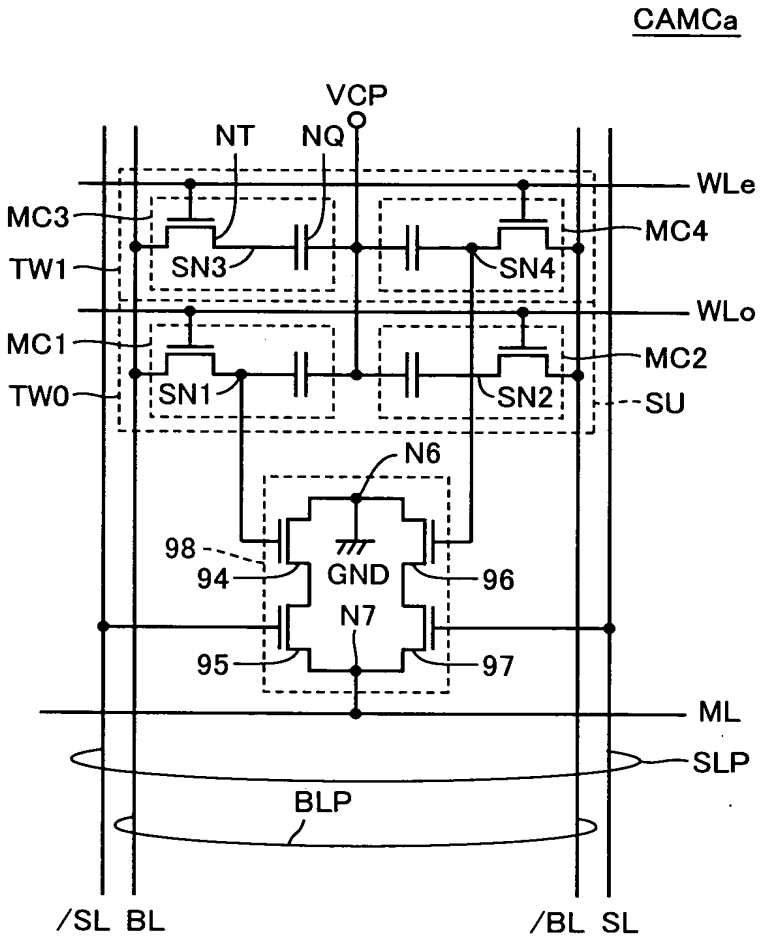

CAMC#
WL
ML
MCUb
MCUa
VCC
GND
GTR
/GTR
SNR
/SNR
GTL
/GTL
SNL
/SNL
BLR
/BLR
BLL
/BLL
BLRP
BLLP
SL
/SL
SLP
96
97
98
N6
N7
94
95

FIG.22


CAMCa
VCP
NT
NQ
WLe
MC3
MC4
TW1
SN3
SN4
WLo
MC1
MC2
TW0
SN1
SN2
SU
N6
98
94
GND
96
N7
95
97
ML
SLP
BLP
/SL BL
/BL SL